discharge process discharges a stored electrostatic charge at a predetermined rate.

41. (Amended) An article of manufacture comprising:

an analog time cell; and

a conductive lead ~~circuitry~~ for allowing a state of the analog time cell to be modified or read.

III. General Remarks Concerning This Response

Claims 1-45 are currently pending. Claims 32 and 41 have been amended in this response.

The cross-reference section of the specification has been amended to change the attorney docket numbers to patent application serial numbers.

The pending Office action has two objections to the drawings. The first objection to the drawings states that Figures 1A-1J should be labeled as "Prior Art". A proposed drawing correction has been submitted with this response that adds a "Prior Art" label to Figures 1A-1J. The second objection to the drawings states that element 328, shown in Figure 3A, is not mentioned in the description. The specification has been amended to mention element 328.

The pending Office action has two objections to the specification. The first objection to the specification states that the time detection unit 230 is incorrectly referred to as element 220 on page 47, line 6. The specification has been amended to correct the noted defect.

The second objection to the specification concerns the term "programming operation"; the Office action states the following on page 4, paragraph 2:

> The disclosure states a "programming operation," which is misdescriptive and is in fact nothing more than a charging operation. Appropriate correction to the numerous instances within the disclosure containing the misdescriptive material is required.

Applicant strongly disagrees that the term "programming operation" is misdescriptive. In the specification, Applicant discusses the modifications that can be made to a non-volatile memory cell to create one embodiment of the present invention, and the verb "to program" is a common term in the prior art associated with non-volatile memory cells.

For support of Applicant's contention, Applicant points to Prince, the first reference in the IDS that Applicant submitted with the present application. In addition to other uses of this terminology, on page 186, each of Figures 5.24(a)-(d) have a label "Program" along with an arrow for showing the flow of charge carriers. On page 185, the text states (emphasis added): "Figure 5.24 shows schematic cross-sections of a series of cells that have been developed for the single cell flash memories showing the range of mechanisms from hot electron **programming** to low voltage cold electron erase and reprogramming."

Applicant can also point to Amin, the third reference in Applicant's IDS, which shows (among numerous other uses of the term "program") on page 373 that Fig. 12 is labeled "Programming characteristics of cell A ..." while stating on

that page (emphasis added): "The **programming** characteristics for cell A are shown in Fig. 12 and 13.".

In addition, Applicant can also point to Chi et al., the last reference in Applicant's IDS, which shows on page 94 (among numerous other uses of the term "program") that Fig. 1 is labeled "Low-voltage **Programming**" while the text states (emphasis added): "This paper proposes true low-voltage operations for **program**, erase, and read in flash memory."

Given that the term "program" is used extensively in the prior art, Applicant asserts that the term "program" has not been used in a way that is repugnant to its ordinary meaning, and Applicant asserts that the present application's terminology would be understood by one having ordinary skill in the art. Applicant declines to change the numerous uses of the term "program" in the specification unless publications can be produced by the Office to show that the objection is factually based and that Applicant's terminology is truly misdescriptive.

With respect to the reasons for the claim amendments, independent claim 32 has been amended to fix an antecedent basis problem. Applicant also notes the following for the record. Since the amended subject matter in amended independent claim 41 was previously presented in substantially the same manner in the originally filed patent application, albeit in a slightly narrower form, Applicant submits that the subject matter of previously presented independent claim 41 has not been substantially amended. Applicant notes that the claim has not been amended for the purposes of avoiding the prior art.

IV. Rejections under 35 U.S.C. § 112, ¶ 2

Claims 41-45 have been rejected under 35 U.S.C. § 112, ¶ 2, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. On page 4, last paragraph, the Office action states:

> The omitted structural cooperative relationships are: a clear definition of the circuitry and the relationship of the circuitry to the time cell in order to allow reading a state of the time cell, as well as a clear structural definition of the smart card and the structural relationship the smart card has to the time cell. Applicant must include a description, illustration, or a previous patent showing the components or features of the said circuitry.

In the specification, Applicant discusses the modifications that can be made to a non-volatile memory cell to create one embodiment of the present invention. In the specification, Applicant also discusses the similarities between reading or programming a non-volatile memory cell and reading or programming a time cell of the present invention. Hence, Applicant asserts that one of ordinary skill in the art would understand that circuitry for reading or programming a time cell of the present invention would be similar to circuitry for reading or programming a non-volatile memory cell.

As a reference for such circuitry, Applicant points to Masuoka et al., "Reviews and Prospects of Non-Volatile Semiconductor Memories", which Applicant submitted as the sixth reference on Applicant's IDS that was submitted with the present application. Fig. 3 in that reference shows a memory cell array with well-known circuitry features, such as a word

line, a select line, and bit lines that allow for operations on individual memory cells within a memory cell array.

However, rather than argue over the term "circuitry", Applicant has broadened the claims by amending independent claim 41 to delete the term "circuitry" and substitute therefor the term "conductive lead". For example, claim 41 now reads: "a conductive lead for allowing a state of the analog time cell to be modified or read". Support for this terminology is found on page 21, lines 3-7, which state:

> Conductive contacts **108** and **110** from the source and the drain, respectively, are insulated from other portions of the device by insulating regions **112** and **114**, respectively, and the conductive leads allow current to flow to or from the source and the drain when appropriate.

In order to show that Applicant has not used the term "conductive lead" in a manner that is repugnant to its ordinary meaning, Applicant has attached to this response a photocopy of page 636 from Whitaker, *The Electronics Handbook*, IEEE Press, 01/1996, which states: "Lead: A conductive path, usually self-supporting, the portion of an electrical component that connects it to outside circuitry".

With respect to the term "smart card", Applicant assumes that the rejection is referring to dependent claim 43, which states "wherein the article of manufacture is a smart card". The specification describes various possible configurations of the present invention within a smart card. For example, on page 52, lines 12-14, the specification states: "Time cell interface unit **320** and time cells **301-316** may reside in a physically separable object, such as a portable device like as a simple, externally powered, smart card." Applicant asserts

that one of ordinary skill in the art would recognize that one could connect a time cell with a conductive lead that, in turn, is conductively connected to some form of circuitry in the smart card.

Given that the claims now recite the term "conductive lead" rather than the term "circuitry", Applicant has addressed the rejection. Although Applicant disputes the argument in the rejection that the original form of the claims has omitted essential structural cooperative relationships, Applicant asserts that there is no longer any logical basis for arguing that the claims omit an essential element, and Applicant requests the withdrawal of the rejection.

Claims 27-31 have been rejected under 35 U.S.C. § 112, ¶ 2, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. On page 5, paragraph 3, the Office action states: "There are no steps for displaying or measuring time, since the methods are drawn to a horological device". Applicant strongly disagrees with the statement that there are no steps for measuring time. Independent claim 27 states: "discharging the stored electrostatic charge from the charge storage element". This discharging process indicates time passage; in other words, it is a step for measuring time.

In contrast to the statement in the rejection, the claims appear to include all that is required to be recognized as associated with an horological device by the Patent Office's own classification definitions, which are part of the Patent Office's subject matter classification system. Class 368 is directed to "Horology: Time Measuring Systems or Devices".

The "general statement of the class subject matter" for Class 368 states: "This class is the generic class for instruments or portions of instruments employed for the measurement of time passage in units of hours, minutes, seconds, or fractions thereof or the like." As described in the specification, the present invention measures time passage in a manner that can be described as an electrostatic hourglass. Hence, Applicant asserts that there is no logical basis for arguing that the claims omit an essential step, and Applicant requests the withdrawal of the rejection.

V. Summary of Present Invention

A simple electronic horological device, termed a time cell, is presented with associated methods, systems, and computer program products. A time cell has an insulated, charge storage element that receives an electrostatic charge through its insulating medium, i.e. it is programmed. Over time, the charge storage element then loses the charge through its insulating medium. Given the reduction of the electric potential of the programmed charge storage element at a substantially known discharge rate, and by observing the potential of the programmed charge storage element at a given point in time, an elapsed time period can be determined. Thus, the time cell measures an elapsed time period without a continuous power source. One type of time cell is an analog time cell that may have a form similar to a non-volatile memory cell, particularly a floating gate field effect transistor (FGFET). The time cell may have an expanded floating gate for storing an electrostatic charge. At a given

point in time after programming the analog time cell, a sensing operation indirectly observes the retained charge in the floating gate by directly or indirectly observing the threshold voltage of the FGFET. By knowing the operational characteristics of the time cell and its initial programming condition, the observation can be converted into an elapsed time value. A time cell can be designed and/or programmed to select the range of time to be measured.

VI. 35 U.S.C. § 103(a)—Obviousness—*Admitted Prior Art in view of Suzuki*

The Office action has rejected claims 1-17, 24, 25, 35, and 38-45 under 35 U.S.C. § 103(a) as unpatentable over Admitted Prior Art in view of Suzuki, U.S. Patent Number 4,442,363, "Timer Switch for Vehicle", issued 04/10/1984. This rejection is traversed.

As a preliminary issue, the logical structure of the rejection is inconsistent. Claims 24 and 25 depend from dependent claim 23, which itself depends on independent claim 18. Claims 24 and 25 have been rejected on the above-noted grounds, yet the independent claim from which they depend have not been rejected under the same grounds. Similarly, claim 35 depends from dependent claim 34, which itself depends on independent claim 32. Claim 35 has been rejected on the above-noted grounds, yet the independent claim from which it depends has not been rejected under the same grounds.

With respect to claims 1-17, 24, 25, 35, and 38-45, the rejection of all of the claims says within multiple statements that the "Admitted Prior Art" teaches a time cell. For

example, on page 6 of the pending Office action, the rejection states: "Regarding 1 and 41-42, the Admitted Prior Art teaches a horological device comprising all of the structural features shown in Figure 1A: ...". This statement is false. The truly admitted prior art does not teach a time cell; a time cell was a novel entity that was disclosed by the present patent application.

The most important point with respect to the patentability of the present invention is that no prior art teaches *an horological device* comprising the recited features. The Office action has not applied any prior art publications against the claims that disclose *an horological device* with the recited features.

Possibly most importantly with respect to the logic of the rejection, Applicant readily admitted in the specification to the similarities between the present invention and the prior art, but Applicant also took great care in distinguishing the present invention from the prior art. Specifically, the specification states on page 39 (emphasis added):

> It is noted that this embodiment of the present invention relies upon various structures, programming operations, reading operations, and erasing operations of non-volatile memory cells comprising charge storage elements that were known and well-established in the prior art. **However, the prior art did not teach the use of a non-volatile memory cell as an horological device.**

Hence, the rejection has asserted something as "admitted" prior art, yet Applicant actually explicitly stated the opposite in the specification. In other words, the truly admitted prior art does not include an horological device with

the recited features. The preamble of the independent claims must be given weight during an interpretation of the claims.

Various elements of the claims seem to have been ignored by the rejection. For example, independent claim 40 contains the following element: "wherein the thickness of the insulating region is selected such that a threshold voltage of the second floating gate field effect transistor has a predetermined decay rate after programming the floating gate". This claim element has not been addressed by the rejection, and Applicant asserts that the claimed feature is not found in the truly admitted prior art.

In fact, the prior art teaches away from this feature because non-volatile memory cells are designed to prevent charge leakage. Applicant specifically explained this in the specification, which states on pages 39-40 (emphasis added):

> **Moreover, in the prior art, charge leakage from the charge storage elements in non-volatile memory cells was viewed as a detrimental nuisance, and if anything, the prior art taught that charge leakage should be avoided and potentially eliminated. The present invention makes the novel observation that the charge leakage rate can be selected in a manner that allows it to be useful.** Using this novel observation, the charge storage element in a non-volatile memory cell can be engineered as an horological device that allows measurements of its operation such that elapsed time periods can be determined. Specifically in this embodiment, as discussed above, the geometry and physical properties of the insulating medium through which the retained electric charge leaks is selected in a manner which controls the leak rate.

Hence, the truly admitted prior art specifically did not "admit" this feature and actually described how the prior art taught away from this feature.

Moreover, the rejection is written as if the term "time cell" was prevalent in the prior art at the time of the present invention, which was not the case. The term "time cell" was coined by the present patent application (and its related patent applications) to distinguish the present invention from prior art memory cells. A patent applicant is allowed to be his/her own lexicographer as long as a term that is used in the claims does not have an art-accepted meaning that significantly differs from the applicant's use of the term and the term is adequately defined in the description. In this case, Applicant asserts that there is more than adequate disclosure and definition in the present patent application for Applicant's insistence that the term "time cell" must be given consideration, particularly when the rejection has apparently not given it any consideration.

Prior to discussing deficiencies in the rejections of individual claims, Applicant discusses a common, important aspect of all of the obviousness rejections in the pending Office action. The rejection states on page 6, last paragraph, to page 7, first paragraph:

> The Admitted Prior Art does not teach the concept of measuring the electrostatic discharge of the charge storage element in order to obtain the corresponding elapsed time of the system. Suzuki teaches a convention RC timer, which teaches the concept of measuring the electrostatic discharge of a charge storage element in order to provide the corresponding elapsed time (Col. 1, lines 12+).

This statement is made with respect to independent claims 1 and 41 and dependent claim 42, but similar statements are made throughout the Office action with respect to obviousness

rejections of other claims. Specifically, all of the obviousness rejections rely on Suzuki for teaching some aspect of the claim language. More specifically, the central argument in the obviousness rejections is that Suzuki teaches a conventional RC timer, and the central argument asserts that a conventional RC timer has characteristics that are equivalent to various characteristics of the present invention.

Applicant asserts that the central argument of the obviousness rejections is incorrect. A conventional RC circuit requires a constant or periodic source of electrical energy, such as a battery, to be able to measure the passage of time, whereas the present invention does not require a battery or similar source of electrical energy.

More importantly, a conventional RC circuit works by discharging the stored charge in one or more capacitors through one or more conductive paths. The conductive plates in a capacitor are directly connected to conductive leads through which a stored charge flows. In contrast, a time cell in the present invention stores an electrostatic charge in an internal medium of a charge storage element, and the internal medium is substantially surrounded by an insulating medium; there are no conductive leads from the internal medium to other elements in a system through which stored charge can flow. Hence, the structure of the present invention is significantly different from a conventional RC timer, and the method of operation is significantly different from an RC timer.

Applicant discussed the operation of conventional capacitors in the specification, and Applicant also took great care in distinguishing the present invention from the prior art. In fact, the specification has an entire section, from page 40, line 16, to page 45, lines 11, devoted to distinguishing the present invention from the prior art that one of ordinary skill in the art might mistakenly conclude teaches the present invention. The section at page 41, line 24, to page 42, line 25, was particularly directed to capacitors; it states:

> A capacitor can store energy, and a resistor placed in series with the capacitor will control the rate at which it charges or discharges, which produces a characteristic time dependence that can be modeled by an exponential function. The crucial parameter that describes the time dependence is the "time constant" RC. The time constant or RC product of a series circuit determines the speed at which the voltage across a capacitor can change. In industry, circuits combining resistors and capacitors are important because they can be used in timing circuits, signal generators, electrical signal shaping and filtering, and a variety of electronic equipment. However, the discharge times of a capacitor are generally very short, usually on the order of milliseconds but possibly a few hours, even when very large capacitors are combined with very large resistances or impedances.

Given that Applicant readily admitted to the existence of RC circuits, and given that the rejection uses Applicant's admissions concerning non-volatile memory cells against Applicant's invention of time cells, it is confusing why the rejection relies on the teachings in Suzuki for the disclosure of a conventional RC circuit rather than using Applicant's truly admitted prior art.

Applicant specifically explained how the present invention is distinguishable from conventional uses of capacitors, RC circuits, etc.; the most significant portion of the specification states on page 44, line 9, to page 45, line 9 (emphasis added):

> Moreover, the prior art does not recognize that the discharge process itself is temporally meaningful for most electrostatic storage devices. **In the case of the capacitor, in which the prior art does recognize that its discharge rate is temporally meaningful, the capacitor is not entirely insulated and only operates through the use of conductive contacts. Moreover, an horologically practical application involving a capacitor is only useful because the discharge process then powers other electrical or electronic components with which it has a conductive contact.** In fact, capacitors are usually employed in a manner which cycles the charging and discharging processes in order to achieve some type of electrical time base. Usually called a relaxation oscillator or a relaxation generator, a fundamental frequency can be generated by the time of charging or discharging a capacitor or coil through a resistor. Hence, capacitors require a continuous power source as they dissipate relatively large amounts of energy for any horological application, which presents a motivating factor for the present invention in which the power source can be eliminated while the electronic horological device continues measuring time.
>
> In contrast to a capacitor, the present invention relies upon a discharge process **wherein an electrostatic charge is discharged from an insulated charge storage element over a period of time in such a manner as to allow one to use the discharge process itself as a temporally meaningful process.** The manner in which the present invention accomplishes time measurement also allows for common, daily activities over potentially long periods of time.

The statement in this response should not be interpreted as showing the only sections in the specification in which the

present invention can be distinguished from the prior art; there are multiple places within the specification in which the novel aspects of the present invention were emphasized.

In light of the extent to which the specification discusses the differences between the present invention and the prior art and the extent to which the rejections rely on well-known RC circuits, Applicant argues that the central argument of the obviousness rejections seems to have completely ignored various characteristics of the present invention. Since the central argument in the obviousness rejections is built on an incorrect conclusion about the similarities between the present invention and the prior art, generally with respect to conventional RC circuits or particularly with respect to the "admitted" prior art and the teachings of Suzuki, either singly or in combination, the obviousness rejections of the claims is improper.

Applicant realizes that concepts about an invention cannot be discussed abstractly without reference to actual claim language. Applicant turns now to particular statements in the rejection of particular claims.

With respect to independent claims 1 and 41 and dependent claim 42, as a preliminary point, Applicant notes that neither independent claim 1 nor independent claim 41 explicitly use the language "measuring the electrostatic discharge of the charge storage element" or similar phrase. While an horological device using the time cell of the present invention may perform this step, this phrase is not contained within these particular claims.

More importantly, the rejection of independent claim 1 has not addressed the following element in the claim:

> wherein the charge storage element comprises an internal medium for storing an electrostatic charge and an insulating medium for insulating the internal medium that substantially surrounds the internal medium, and wherein the time cell transitions from a non-time-measuring state to a time-measuring state in the horological device upon receiving the electrostatic charge;

It may be possible that the rejection of independent claim 1 has not addressed this element in the claim because it was focused on the above-noted phrase that is not contained within claim 1. However, because the rejection has not addressed an important element of independent claim 1, either by reference to the Admitted Prior Art or Suzuki, the rejection of independent claim 1 and its dependent claims is improper for failing to explain how the prior art taught this feature.

With respect to independent claim 41, the claim language uses the term "analog time cell", as opposed to the term "binary time cell" that is used within the claims of a related patent application to claim an alternative embodiment of the present invention. The rejection has not made any attempt to explain how the concept of a "analog time cell" was known in the prior art before the present invention. Using the same argument as presented above, Applicant asserts that the novel terminology of the present application must be considered when interpreting the claims. Given that the rejection has not address this claimed feature, either by reference to the Admitted Prior Art or Suzuki, the secondary reference, the rejection of independent claim 41 and its dependent claims is

improper for failing to explain how the prior art taught this feature.

With respect to independent claims 1 and 46 and dependent claim 47, the rejection relies on Suzuki for disclosing "measuring the electrostatic discharge of the charge storage element". Although this phrase does not appear in these claims, as mentioned above, the present invention is distinguishable from a conventional RC timer, as argued above.

Applicant also takes exception with the motivational statement for combining the Admitted Prior Art and Suzuki. The rejection states on page 7, paragraph 1:

> It would have been obvious to a person skill in the art at the time of the invention to adapt the Admitted Prior Art to form a capacitive timing system comprising existing structures with the ability to measure electrostatic discharge, as taught by Suzuki, in order to measure elapsed time. Both the Admitted Prior Art and Suzuki possess a charge storage element that provides an electrostatic discharge and the ability to read this discharge and provide a corresponding elapsed time is an existing teaching provided by Suzuki. By applying the existing concept of reading the electrostatic discharge of a generic charge storage element of Suzuki to the Admitted Prior Art, elapsed time results could be determined in the same manner only for any different structural source of the electrostatic discharge.

Applicant asserts that the argument for combining the references is completely confusing. In the rejections of claims 1-17, 24, 25, 35, and 38-45, the Admitted Prior Art is the primary reference, and Suzuki is the secondary reference. In a typical obviousness rejection, the primary reference is modified to include a feature that is taught by the secondary reference. In the present obviousness rejection, it is

entirely unclear what feature from which reference is being combined with what other feature.

The rejection states that the Admitted Prior Art could be adapted "to form a capacitive timing system comprising existing structure with the ability to measure electrostatic discharge, as taught by Suzuki, in order to measure elapsed time." Assume *arguendo* that a time cell of the present invention is disclosed by the Admitted Prior Art as argued by the rejection. If the rejection is arguing that the time cell supposedly disclosed in the Admitted Prior Art could be modified to include a feature from the system of Suzuki, then it is unclear why one would be motivated to add a feature to the time cell "in order to measure elapsed time"; the time cell already measures elapsed time, so it is entirely unclear why one would be motivated to add some feature from the secondary reference that is already present in the primary reference. If the rejection is arguing that the system of Suzuki could be modified to include a time cell as supposedly disclosed in the Admitted Prior Art, the RC circuit already measures elapsed time, so it is entirely unclear why one would be motivated to add some feature from the primary reference that is already present in the secondary reference.

Moreover, it is entirely unclear what characteristic of the system of Suzuki is discussed by the rejection. More specifically, the rejection fails to state to what extent the RC timer circuit from Suzuki is being discussed. For example, it is unclear which elements of the system, such as the resistor R, the capacitor C, the transistor Tr, the diode D, either singly or in combination, are being discussed. Then,

depending on which elements are being referenced by the rejection, it is unclear how those elements would be connected to a time cell as supposedly disclosed in the Admitted Prior Art.

In addition, the circuit that is shown in Suzuki requires the use of conductive leads that are connected to the capacitor, i.e. the charge storage element. The rejection does not explain how the circuit in Suzuki would operate with the time cell as supposedly shown in the Admitted Prior Art, which uses conductive leads that are not connected to the internal medium that stores the electrostatic charge.

The central argument of the rejection, i.e. that the RC timer circuit of Suzuki is to be combined in some manner with the time cell of the present invention, would completely negate the advantages of the present invention, thereby rendering it useless. Moreover, the combination of features would completely change the principle of operation of the time cell of the present invention. However, MPEP § 2143.01 states the following:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie obvious*. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Applicant asserts that the motivation for combining the references is not logically consistent, and Applicant also asserts that it would not have been obvious to combine the references when doing so requires a change in the principle of operation of the features that are supposedly disclosed in the Admitted Prior Art.

With respect to dependent claims 2-4, which states that the predetermined discharge rate of the discharge process has particular characteristics, the rejection also refers to the RC timer circuit of Suzuki. The same arguments that were presented above by Applicant against the rejection of claim 1 are also applicable to claims 2-4.

With respect to dependent claims 5-7, which includes the feature in claim 5 of "an array of time cells" and the feature in claim 6 of "wherein at least one time cell in the array of time cells has a predetermined time period that differs from a predetermined time period of another time cell in the array of time cells", the rejection has used a principle from *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). The rejection states that the claimed features are "mere duplication of parts for a multiplied effect". First, it is unclear what would be meant by a "multiplied effect" in the feature that is claimed in claim 6. Second, Applicant disagrees that the feature is a mere duplication of parts as each array in the time could measure a different time period; hence, the time cells would not be duplicates of each other, which the argument in the rejection fails to consider.

With respect to claims 8, 9, 24, and 25, which recite various features such as a time cell interface unit and a programming request processing unit, the rejection states that "any capacitive timing device must inherently possess the structure and means to charge/discharge time cells". First, Applicant argues that the statement in the rejection seems to equate all capacitive timing devices with time cells. As already argued above, the novel term "time cell" was defined

in the present patent application, and the term has not been properly interpreted in the rejections, including the rejection of claims 8, 9, 24, and 25. A conventional RC circuit, no matter what its structure is, is not a time cell. Second, the rejection improperly uses an inherency argument by stating: "It would have been obvious to a person skill in the art at the time of the invention to recognize that any capacitive timing device must inherently possess the structure and means to charge/discharge time cells, ...". It is entirely possibly for the claimed features to be included in a second device that interfaces with a first device, as described in the specification. Hence, Applicant asserts that the rejection must refer to another reference for these features since they are not found in the truly admitted prior art nor Suzuki.

With respect to claims 10-13, 38, and 39, which focus on methods of programming and discharging a time cell, the rejection states that "the combined teachings of the Admitted Prior Art and Suzuki inherently possess" these methods. Again, Applicant argues that the statement in the rejection seems to equate all capacitive timing devices with time cells. As already argued above, the novel term "time cell" was defined in the present patent application, and the term has not been properly interpreted in the rejections. In addition, this rejection again misuses an inherency argument. As noted above, the rejection does not describe the manner in which the elements in the circuit of Suzuki are interfaced with a time cell as supposedly disclosed in the Admitted Prior Art, so it is not possible for one having ordinary skill in the art to

discern whether the combined structure does or does not have the resulting qualities from which one having ordinary skill in the art could factually argue that the combined structure truly has the claimed features or properties.

With respect to claims 14-17 and 40, which focus on a computer program product for using an horological device that comprises a time cell, the rejection merely relies on the rejection of other claims. Applicant maintains that the arguments that were presented above with respect to other claims are also applicable to these claims.

With respect to dependent claim 35, which states that the selected thickness of the tunneling region is less than 7 nanometers, the rejection improperly applies the term "tunneling region" to a typical RC timer circuit. The rejection states on page 10, paragraph 1: "By applying a typical RC timer circuit characteristics regarding thickness of the insulation region, the electrostatic discharge of a charge storage element can be controlled." The entire argument appears to illogically discuss a tunneling region of a floating gate transistor with respect to capacitive plates in an RC timer circuit. The rejection merely jumps to an illogical conclusion; Applicant asserts that the claimed feature is not shown in the prior art nor could one apply the teachings of one reference to the other in the manner that is described by the rejection.

With respect to dependent claim 43, which recites that the time cell of the present invention could be used in a smart card, the rejection states that the combination of the Admitted Prior Art and Suzuki does not disclose this feature,

but then the rejection jumps to the conclusion that it would have been obvious to have the feature. Applicant asserts that the rejection improperly uses Applicant's own teachings against the claimed invention.

With respect to dependent claims 44-45, which recites coupling means and timer determining means, the rejection states that the combination of the Admitted Prior Art and Suzuki does not disclose these features, but then the rejection jumps to the conclusion that it would have been obvious to have such features. Again, Applicant asserts that the rejection improperly uses Applicant's own teachings against the claimed invention. In addition, this rejection again misuses an inherency argument. As noted above, the rejection does not describe the manner in which the elements in the circuit of Suzuki are interfaced with a time cell as supposedly disclosed in the Admitted Prior Art, so it is not possible for one having ordinary skill in the art to discern whether the combined structure does or does not have the resulting qualities from which one having ordinary skill in the art could factually argue that the combined structure truly has the claimed features or properties.

Examiner bears the burden of establishing a *prima facie* case of obviousness.

The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Only when a *prima facie* case of obviousness is established does the burden

shift to the applicant to produce evidence of nonobviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). In response to an assertion of obviousness by the Patent Office, the applicant may attack the Patent Office's *prima facie* determination as improperly made out, present objective evidence tending to support a conclusion of nonobviousness, or both. *In re Fritch*, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

With respect to the claims, the rejection argues that a combination of the Admitted Prior Art and Suzuki discloses the claims, but Applicant has shown above that the Admitted Prior Art and Suzuki, either singly or in combination, do not disclose the claimed features. The rejection also has not properly interpreted terms within the claim language, and the rejection has incorrectly concluded that Applicant has admitted to certain features as prior art. Moreover, the rejection has used logically inconsistent arguments, and in addition, the rejection has improperly used Applicant's own teachings against the claimed invention. Hence, the rejection does not establish a *prima facie* case of obviousness with respect to claims 1-17, 24, 25, 35, and 38-45. Therefore, the rejection of these claims under 35 U.S.C. § 103(a) has been shown to be improper, and these claims are patentable over the

applied reference. Applicant requests the withdrawal of the rejection.

VII. 35 U.S.C. § 103(a)—Obviousness—*Admitted Prior Art*

The Office action has rejected claims 18-23, 26-34, 36, and 37 under 35 U.S.C. § 103(a) as unpatentable over Admitted Prior Art. This rejection is traversed.

With respect to independent claims 18-23 and 26, the rejection states the following:

> The combination [sic--it should read "Admitted Prior Art" instead of "combination" because Suzuki is not part of the grounds of rejection] does not explicitly teach an electrostatic detector physically coupled to the charge storage element for allowing a detection of an electrical potential within the internal medium. It would have been obvious to a person skilled in the art at the time of the invention to recognize that the Admitted Prior Art comprises read operations that provide a read operation voltage, which is analyzed in order to provide an indication that the floating gate has been charged, therefore in essence detecting an electrical potential within the internal medium and processing the information. By stating that an electrostatic detector is included in the invention, the claims are restating existing read operation and subsequent data interpreting steps in the Admitted Prior Art.

With respect to claim 18, Applicant agrees with the rejection that Applicant's truly admitted prior art does not teach the claimed features, particularly "wherein at least one physical property of the insulating medium has been selected so that the discharge process discharges a stored electrostatic charge at a predetermined discharge rate", as required by the claim language of claim 18.

However, the rejection improperly uses the Applicant's own disclosure in jumping to a conclusion that the present invention would have been obvious. As already explained above, the prior art teaches away from this feature because non-volatile memory cells are designed to prevent charge leakage; Applicant specifically discussed this in the specification. The motivational statement in the rejection seems to rely on circular reasoning as if saying that it would have been obvious because it should have been obvious. Applicant maintains that the rejection cannot use Applicant's own disclosure against the claimed invention.

With respect to claims 27-31, the rejection states the following (no particular claim is discussed in this rejection as they are grouped together):

> The Admitted Prior Art does not explicitly teach the method for using a horological device comprising the above stated characteristics. It would be obvious [sic--wrong tense] to a person who is skilled in the art at the time of the invention to recognize that because the Admitted Prior Art teaches all of the necessary structure, the methods of charging a charge storage element within controlling electrostatic discharge during and after discharging and charging states of a time cell [sic] in order to gain measurement of the elapsed time of the system and the corresponding charging and read operation steps needed to initialize and process the information of the apparatus are inherently possessed within said structure.

With respect to claim 27, Applicant agrees with the rejection that Applicant's truly admitted prior art does not teach the claimed features, particularly "wherein at least one physical property of the insulating medium has been selected so that the discharge process discharges a stored electrostatic charge

at a predetermined rate", as required by the claim language of claim 27.

However, the rejection improperly uses hindsight and the Applicant's own disclosure in jumping to a conclusion that the present invention would have been obvious. As already explained above, the prior art teaches away from this feature because non-volatile memory cells are designed to prevent charge leakage; Applicant specifically discussed this in the specification. The motivational statement in the rejection seems to rely on circular reasoning as if saying that it would have been obvious because it should have been obvious. Applicant maintains that the rejection cannot use Applicant's own disclosure against the claimed invention.

With respect to claims 32-34 and 36, the rejection states the following (no particular claim is discussed in this rejection as they are grouped together):

> The Admitted Prior Art discloses the claimed invention except for a second source region, a second drain region, a second channel region between the source region and the drain region, and a second control gate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide multiple locations of electrostatic discharge in order to increase acquired data, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Applicant notes that the claimed elements are not merely duplicated. The rejection has completely overlooked one of the claimed features in independent claim 31 (emphasis added):

a floating gate, **wherein a first portion of the floating gate is between the first control gate and the first channel region and a second portion of the floating gate is between the second control gate and the second channel region;**

A similar structure is present in independent claim 36. The rejection has completely failed to address why this particular structure would have been obvious.

With respect to the claims, the rejection argues that the Admitted Prior Art discloses some of the claimed features, but Applicant has argued that the Admitted Prior Art does not disclose certain claimed features. Moreover, the rejection has improperly used hindsight and Applicant's own disclosure against the claim language. Hence, the rejection does not establish a *prima facie* case of obviousness with respect to claims 18-23, 26-34, 36, and 37. Therefore, the rejection of these claims under 35 U.S.C. § 103(a) has been shown to be improper, and these claims are patentable over the applied reference. Applicant requests the withdrawal of the rejection.

VIII. Conclusion

It is respectfully urged that the present application is patentable, and Applicant kindly requests a Notice of Allowance.

For any other outstanding matters or issues, the examiner is urged to call or fax the below-listed telephone numbers to expedite the prosecution and examination of this application.

DATE: August 28, 2002

Respectfully submitted,

Joseph R. Burwell
Reg. No. 44,468
ATTORNEY FOR APPLICANT

Law Office of Joseph R. Burwell
P.O. Box 28022
Austin, Texas 78755
Voice: 866-728-3688 (866-PATENT8)
Fax: 866-728-3680 (866-PATENT0)
Email: joe@burwell.biz

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DIE separation: Refers to the separation of the actual microcircuit chip from the inside of the package.

Destructive physical analysis (DPA): Devices are opened and analyzed for process integrity and workmanship.

Electrostatic discharge (ESD): The instantaneous transfer of charges accumulated on a nonconductor to a conductor, into ground.

Failure in time (FIT): A rating equal to the number of failures in one billion (10^9) h.

Frit: A relatively low softening point material of glass composition.

Function test: A check for correct device operation generally by truth table verification.

Hermetic: Sealed so that the object is gas tight (usually to a rate of less than 1×10^{-6} cc/s of helium.)

Joint Army Navy (JAN): When used when referring to microcircuits indicated a part fully qualified to the requirements of MIL-M-38510 for ICs (now replaced by MIL-M-38535) and MIL-S-19500 for semiconductors. JAN class B microcircuit level of the standard military drawing (SMD) program is the preferred level for design in new weapons systems.

JANTX: A prefix denoting that the military specification device has received extra screening and testing, such as an 100% 168-h burn-in.

JANTXV: A JANTX part with an added precapsulation visual requirement.

Joint Electron Device Engineering Council (JEDEC): A part of the EIA.

Lead: A conductive path, usually self-supporting, the portion of an electrical component that connects it to outside circuitry.

Lead frame: The metallic portion of the device package that makes electrical connections from the die to other circuitry.

Mask: The stencil of circuit elements through which light is shown to expose that circuit pattern onto a photoresist coating on the chip (die). The exposed areas are stripped away leaving a pattern.

Metallization: The deposited thin metallic coating layer on a microcircuit or semiconductor.

Passivation: The process in which an insulating dielectric layer is formed over the surface of the die. Passivation is normally achieved by thermal oxidation of the silicon and a thin layer of silicon dioxide is obtained in this manner. Other passivation dielectric coatings may also be applied, such as silicon glass.

Particle impact noise detection testing (PIND): A test where cavity devices are vibrated and monitored for the presence of loose particles inside the device package via the noise the material makes. These loose particles may be conductive (such as gold flake particles from gold eutectic die attachment operations) and could result in short circuits. This is not required on a 100% basis for military class B devices. It is required for all class S, or devices generally required for spacecraft application use.

Popcorning: A plastic package crack or delamination that is caused by the phase change and expansion of internally condensed moisture in the package during reflow soldering, which results in stress the plastic package can not withstand.

Parts per million (PPM): The number of failures in 10^6 h. A statistical estimation of the number of defective devices, usually calculated at a 90% confidence level.

Schmoo plot: An X–Y plot giving the pass/fail region for a specific test while varying the parameters in the X and Y coordinates.

Soft error: An error, or upset in the output of a part (usually applies to memory devices for a single bit output error), which does not reoccur (i.e., the device performs to specifications when tested after the failure occurred).

Substrate: The supporting material upon which the microcircuit (IC) is fabricated, or in hybrids the part to which the IC (and other components, etc.) is attached.

Tin whisker: A hairlike single crystal growth formed on the metallization surface.

Wire bond: A wire connection between the semiconductor die bond pad and the leadframe or terminal.

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